Jet Propulsion Laboratory
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Results from Recent Thermal Interface/Package on Package/Flip Chip on Board Efforts and Future Packaging Roadmap

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Acknowledgment:

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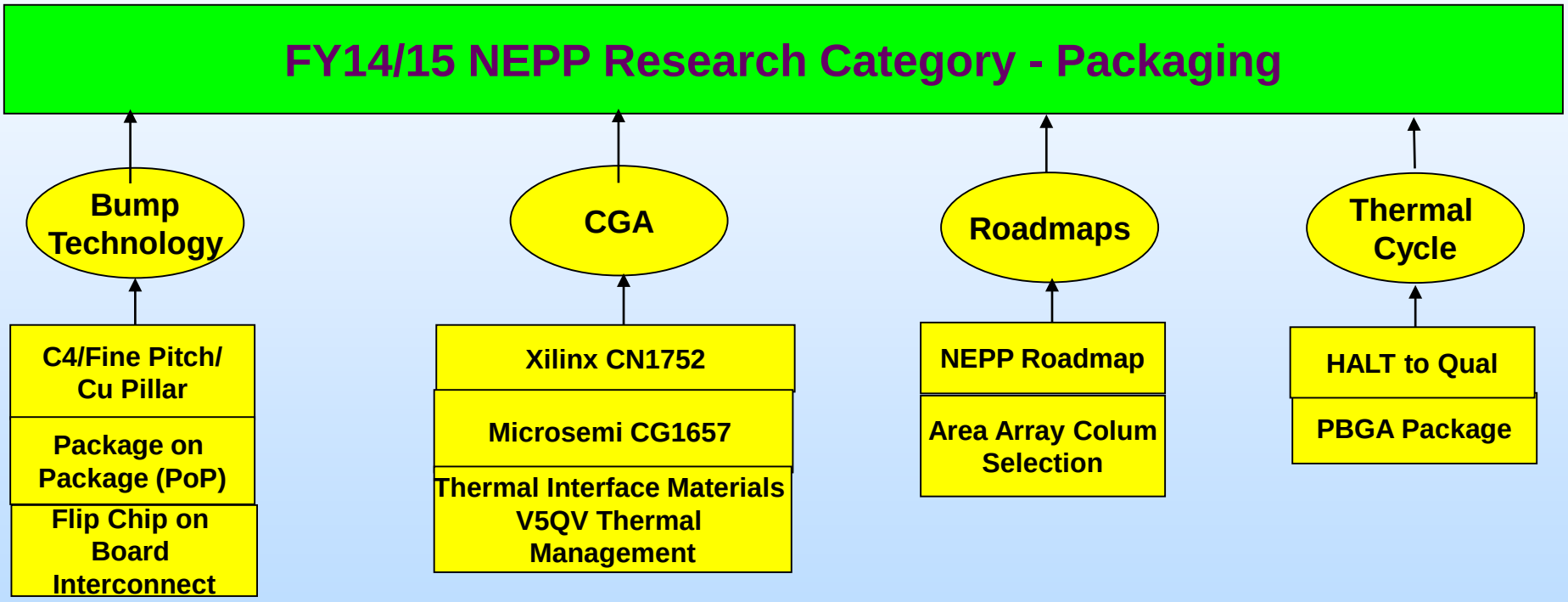
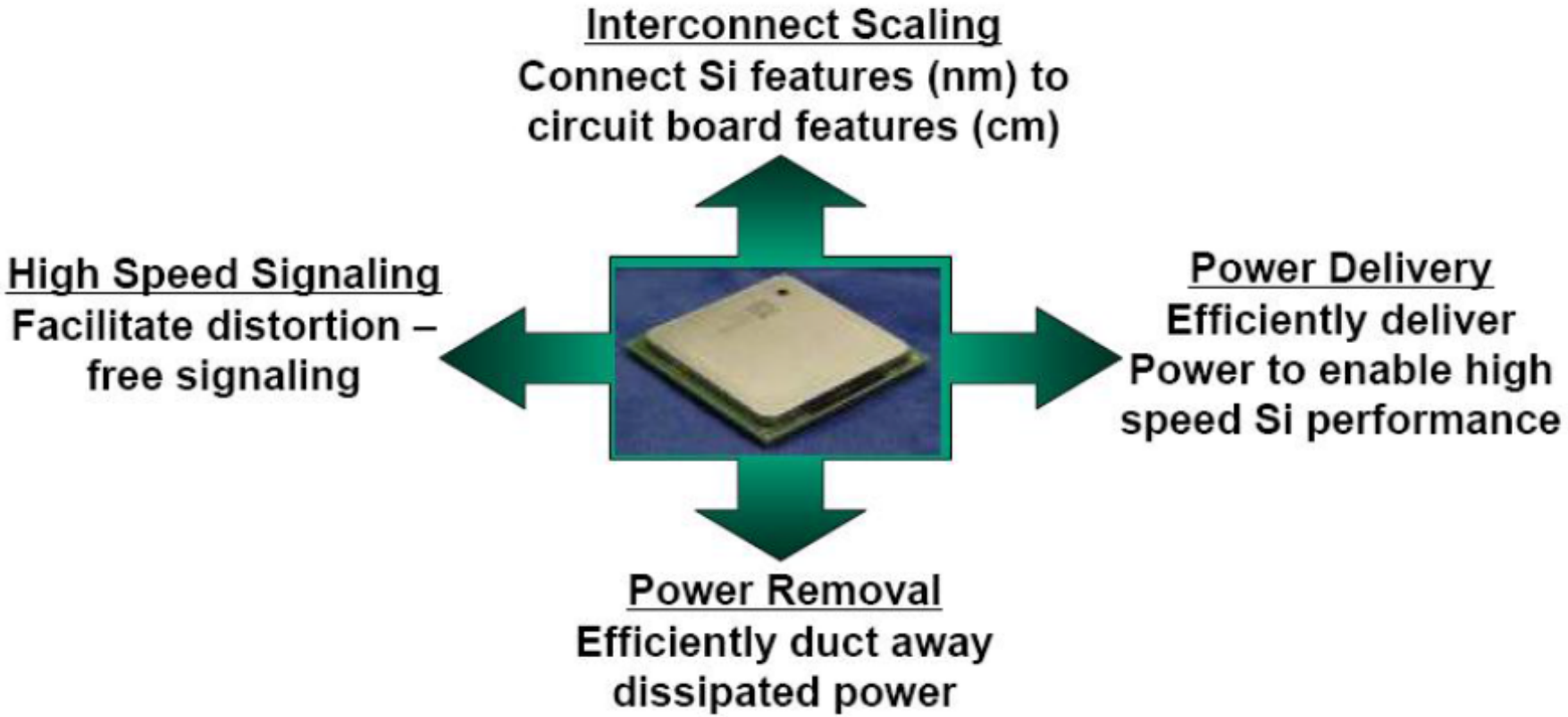
FY14/15 NEPP Research Category - Packaging



NEPP Packaging Tasks

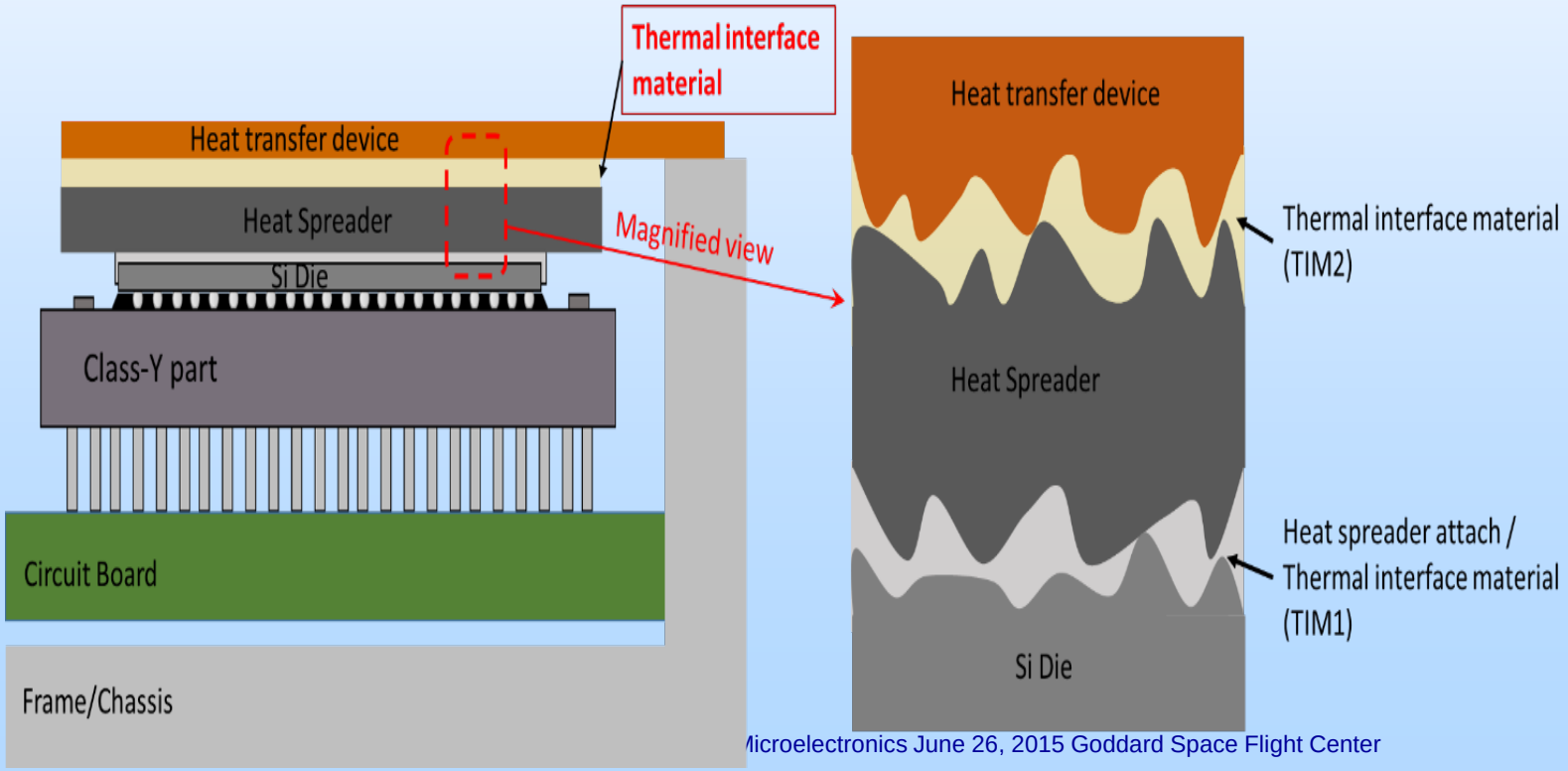
- **Thermal Interface Materials Selection:**
  - **(Jong-ook Suh, Peter Dillon, Steve Tseng)**
- **Package On Package:**
  - **(Peter Dillon, Don Hunter, Atul Mehta, Jong-ook Suh)**
- **Flip Chip on Board:**
  - **(Jong-ook Suh)**

Role of Packaging

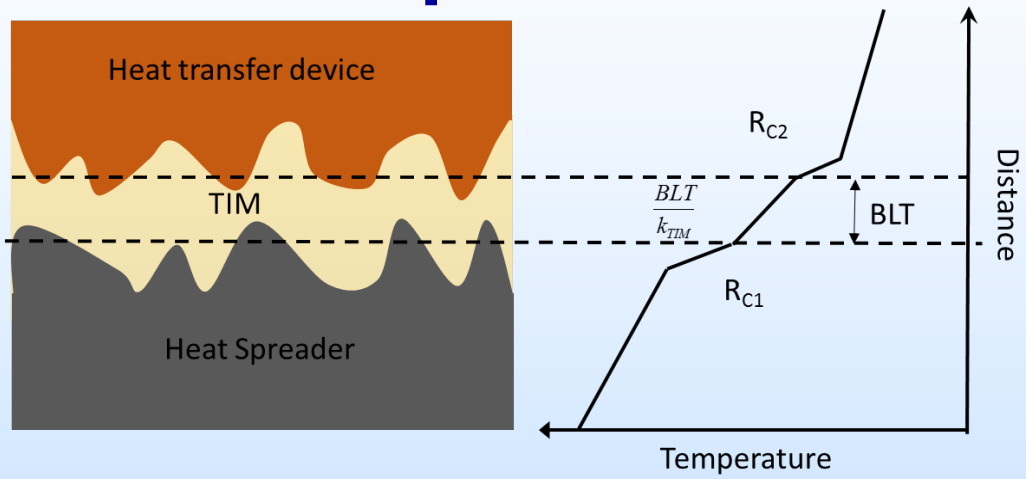


Thermal Interface Materials Selection and Application Guidelines

- **With Perspective to Xilinx Virtex-5QV Thermal Management : $R_{\Theta heat\ spreader} = 0.03 * R_{\Theta board}$**



Thermal Conductivity vs. Thermal Impedance



$$R_{TIM} = BLT / k_{TIM} + R_{C1} + R_{C2}$$

- **Total thermal impedance = TIM's bulk thermal conductivity, bond line thickness, and thermal contact resistances.**
- **In order to achieve low thermal impedance, a TIM needs have high thermal conductivity, low bond line thickness, and low contact resistance.**

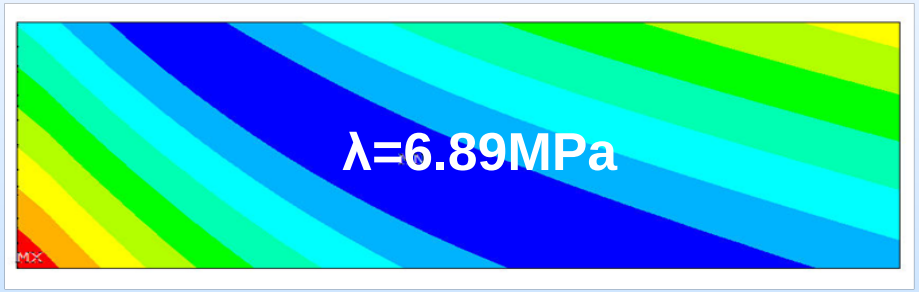
$$R_{TIM} = BLT / k_{TIM} + R_{C1} + R_{C2}$$

- **Bond line thickness can be controlled by adding filler particles**
  - **High concentration of filler can result in increased/uneven bond line thickness and poor contact resistance.**
- **Trade off thickness conductivity and temp cycle reliability**
- **TIMs are characterized per ASTM D5470**
  - **Measures the steady-state thermal impedance and the bond line thickness of a TIM while applying a controlled amount of pressure.**
  - **Does not account for the actual situation where the electronic assemblies are exposed to shock, vibration, and thermal cycling.**

Elastic Modulus

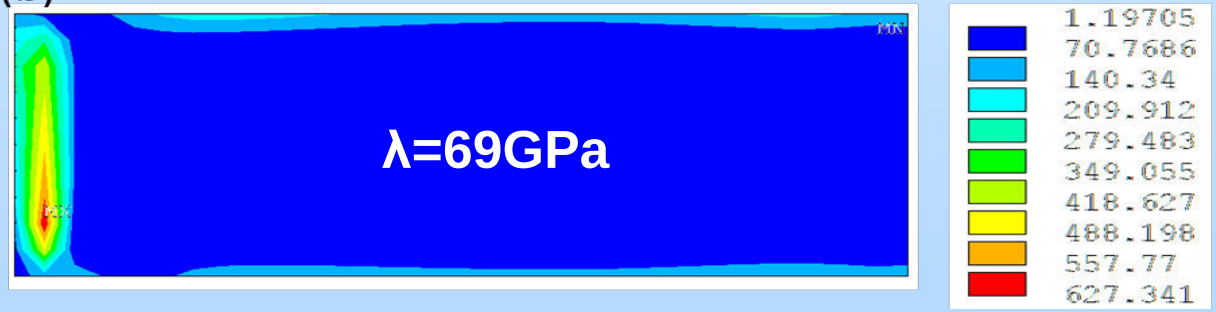
- **Sheer Stress during random vibration test**
- **If the maximum shear stress exceeds the adhesive strength of the TIM, delamination of TIM will initiate**

(a)

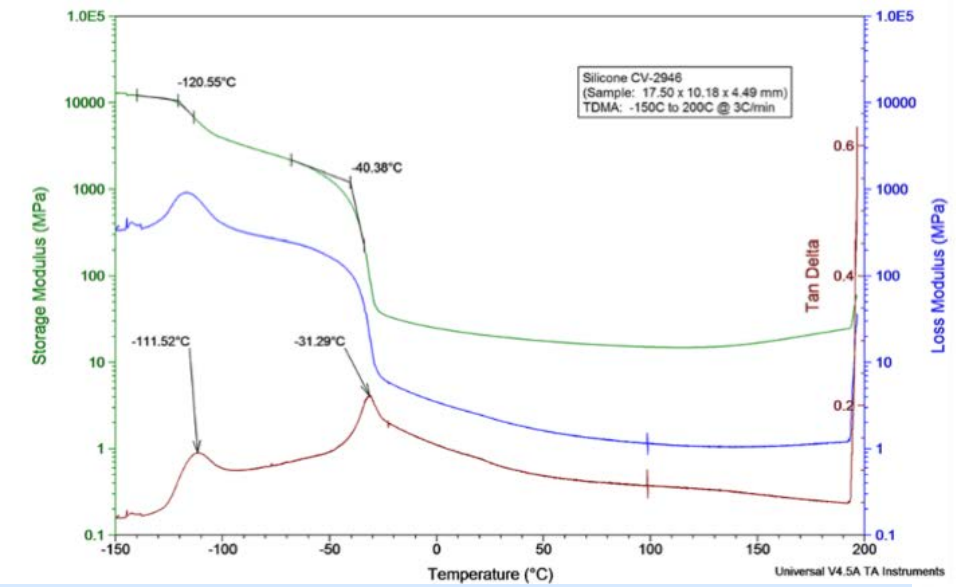


maximum shear stress

(b)

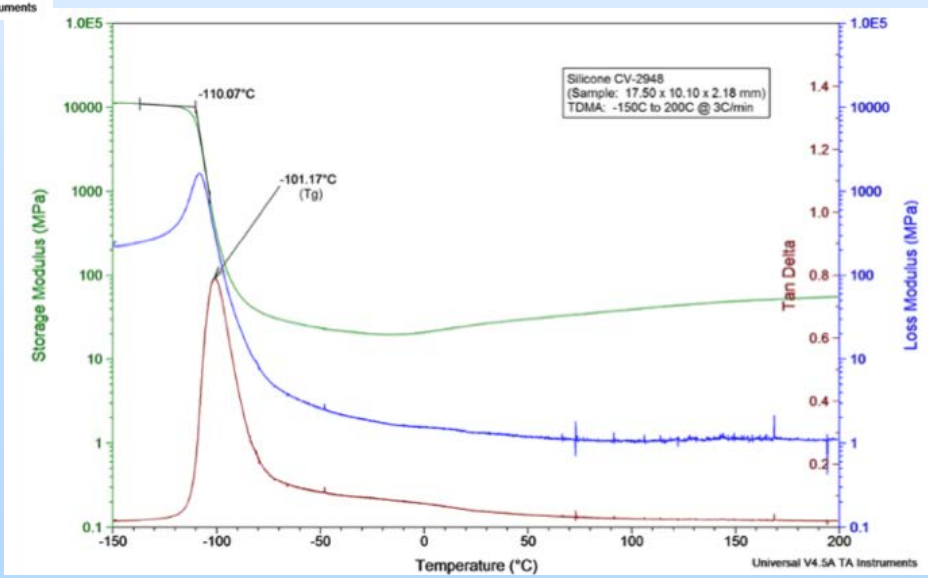


Thermally Conductive Silicones

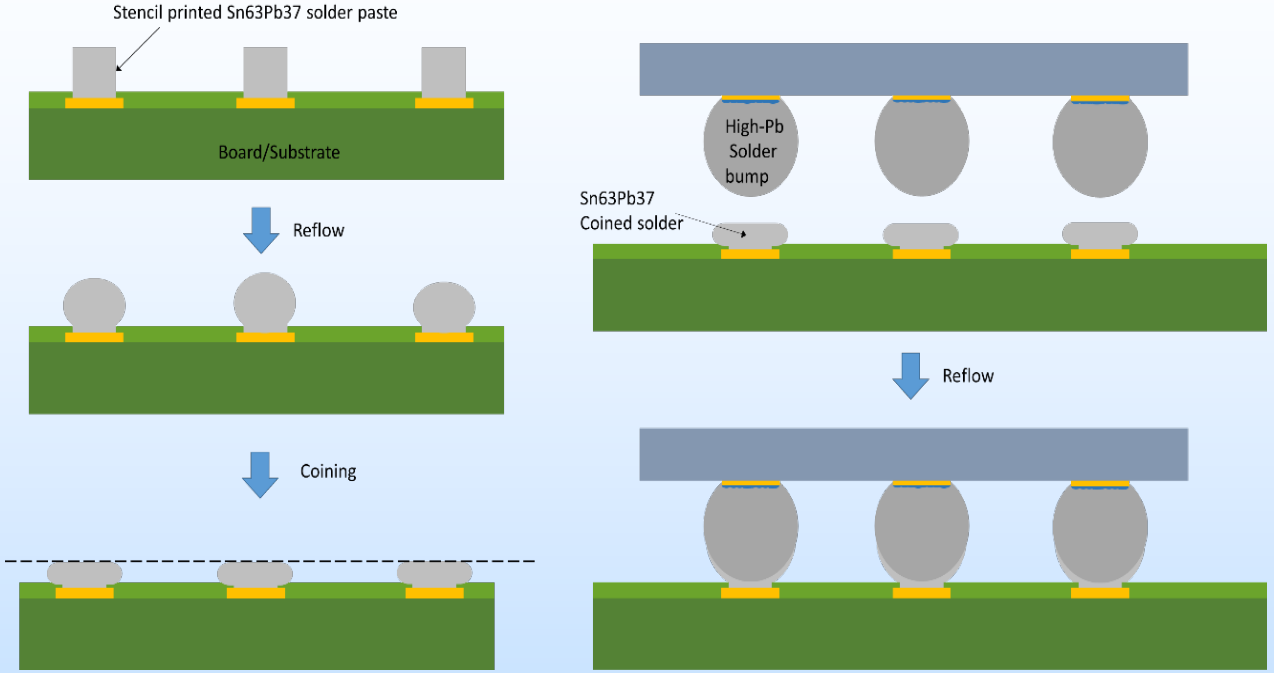


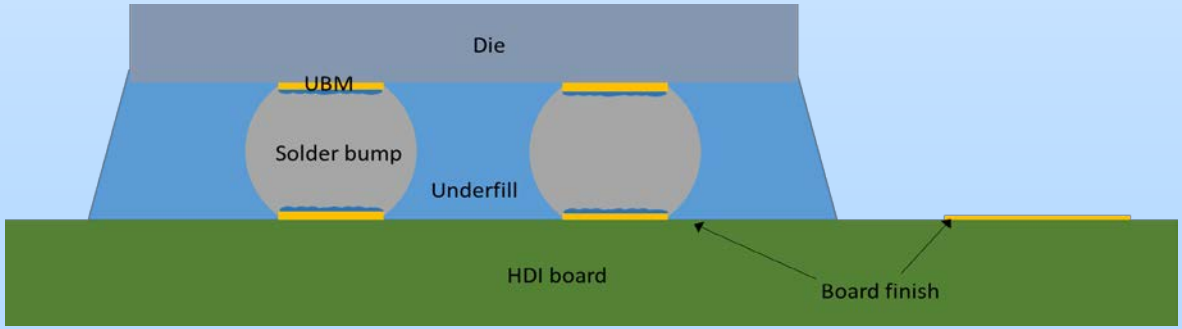
Property	CV-2946	CV-2948	units
Specific Gravity	1.53	1.57	
Durometer	75	80	
Tensile Strength	1.38	1.7	M Pa
Elongation	30	30%	
Tear Strength	50	45	ppi
Lap Shear	1.1	1	M Pa
Thermal Conductivity	1.49	1.95	W/mk
Young's Modulus	20.7		M Pa
Dieletric Strength	21.3		kV/mm

- Similar data sheet specs but different thermal response
- Storage (Elastic) Modulus and Loss (Viscous) Modulus
- Tangent delta is ratio



Flip Chip on Board (FCOB)





FCOB
Material and Reliability Concerns

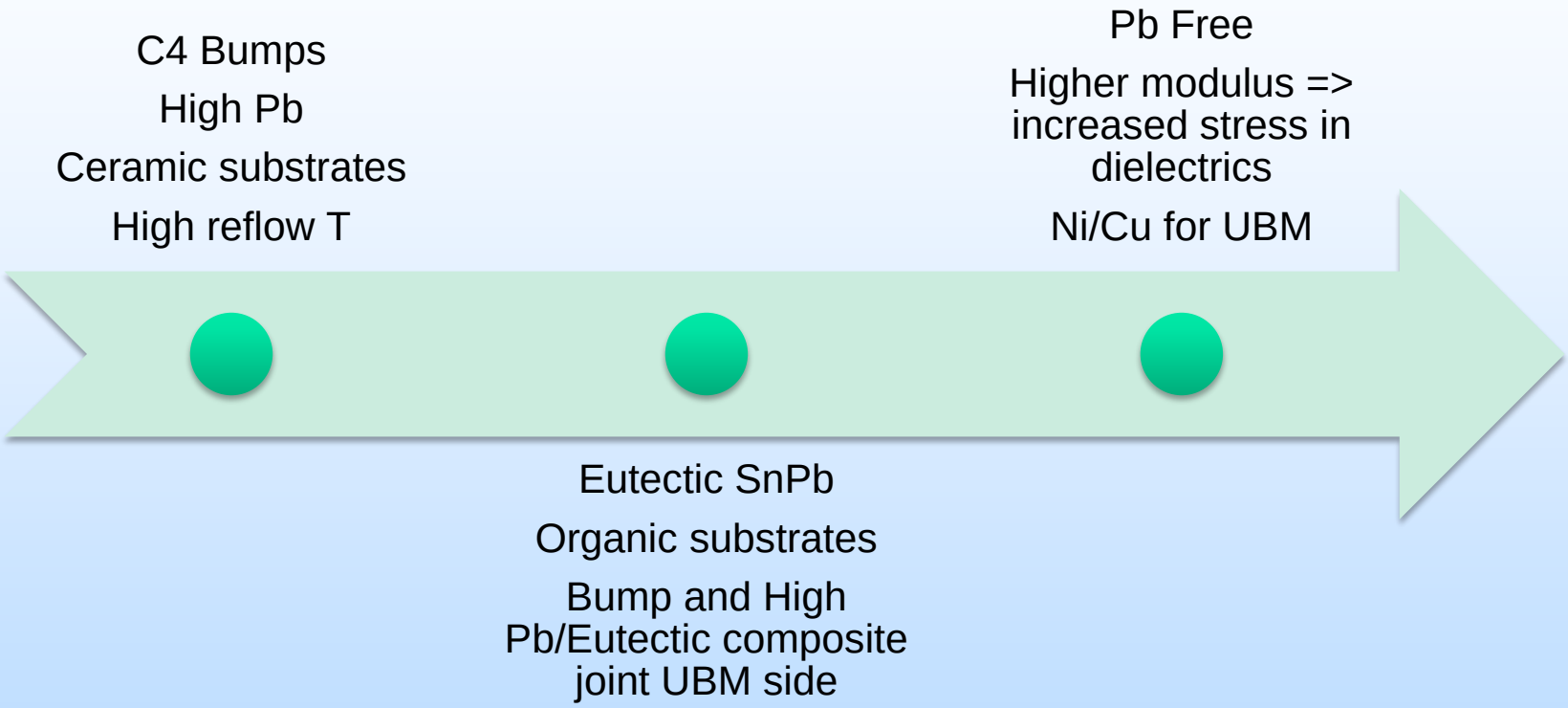
Materials

- Board materials
- Solder bump
- Die metallization
- Board metallization
- Underfill
- Pb-free bumps

Reliability

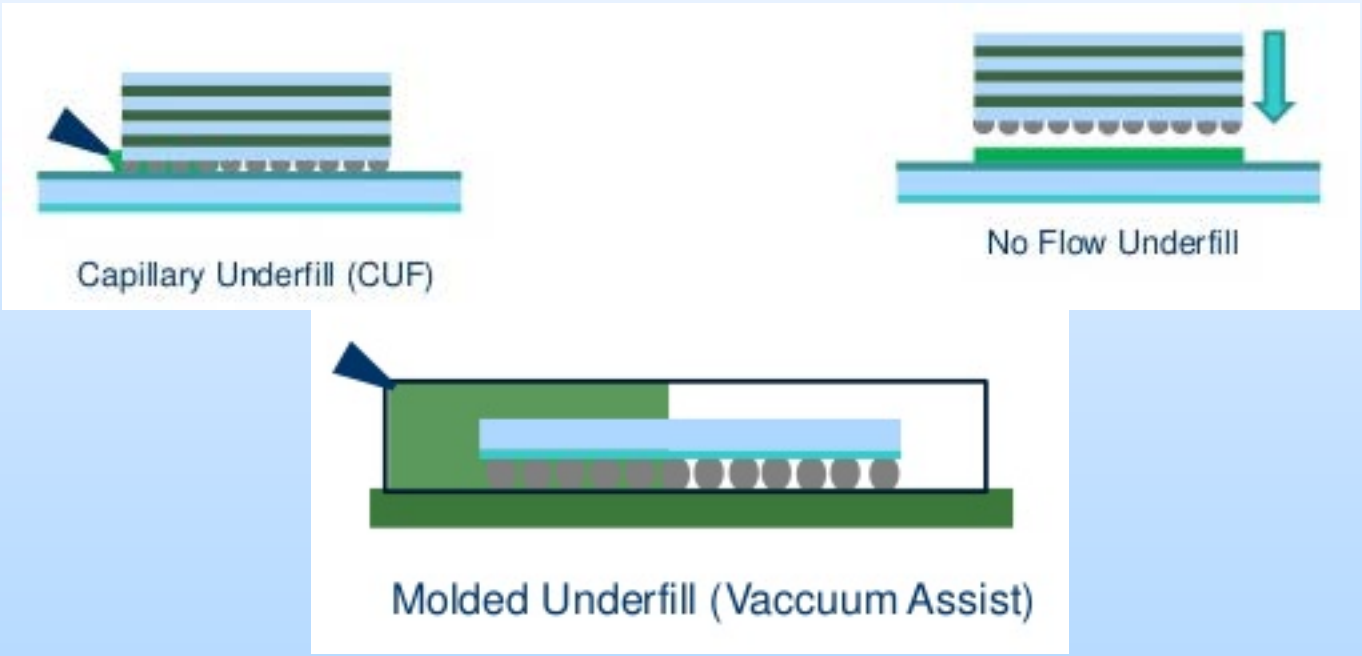
- Dielectric layer cracking
- Metallization/solder reactions
- Thermal Cycle
- Shock/vibe
- Heat dissipation

Bump Evolution

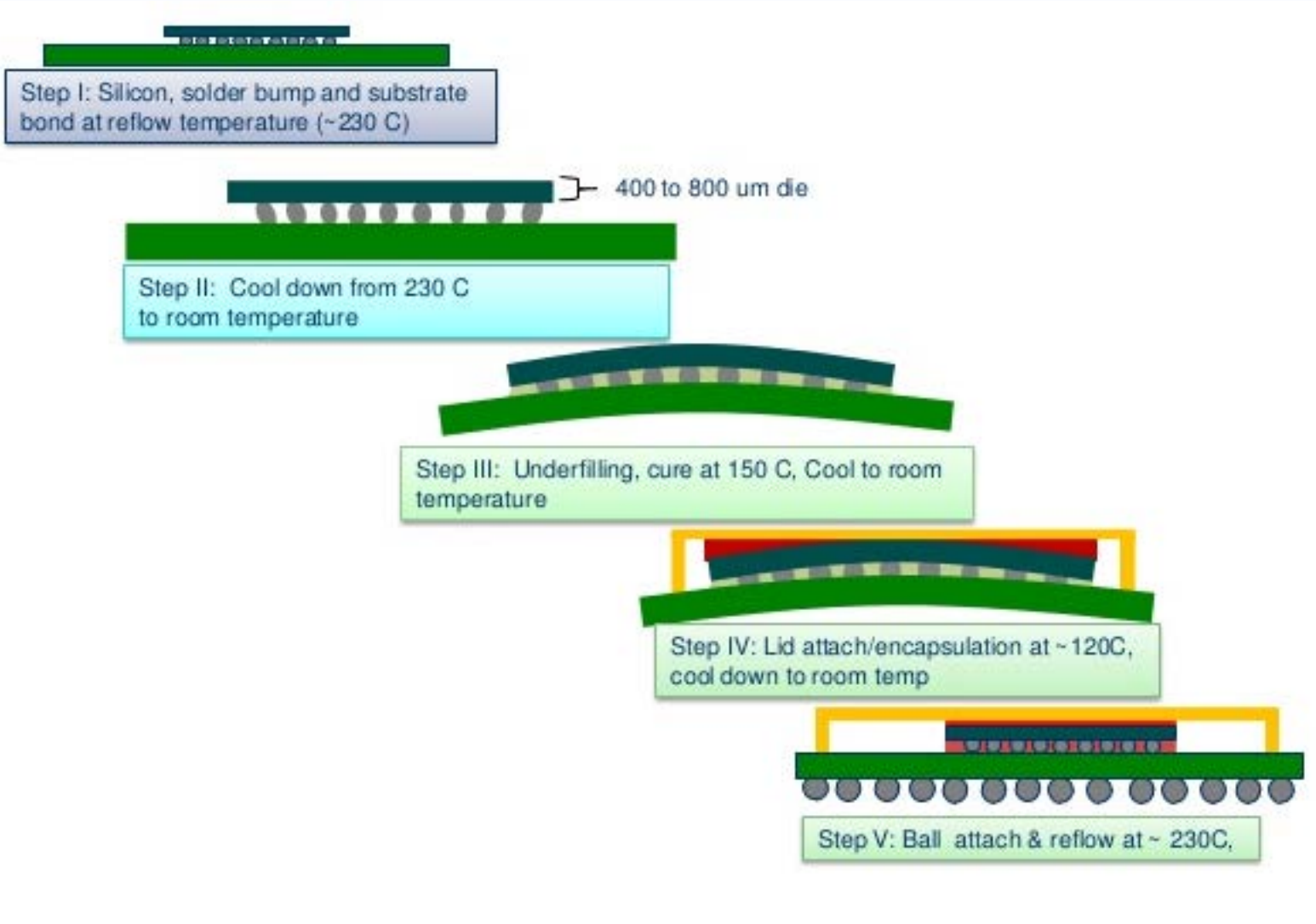


Underfill

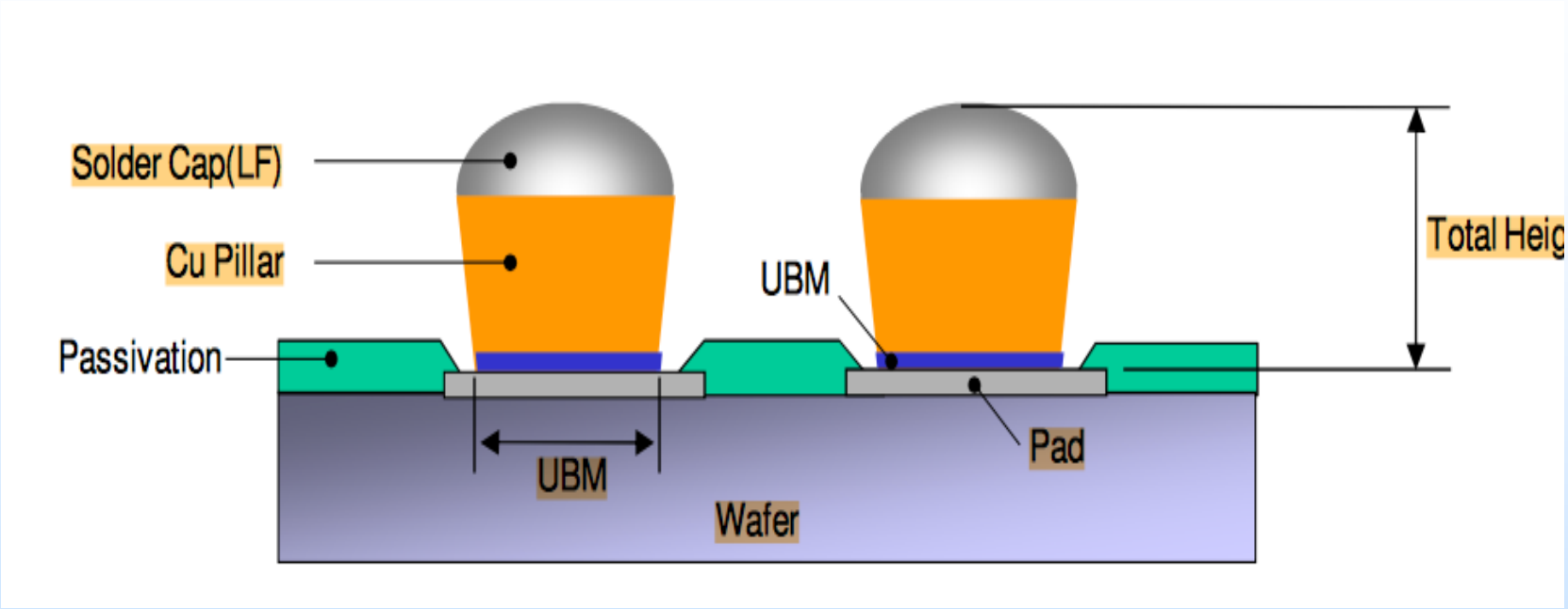
- Silicon die has a CTE of 3 ppm/°C
- Organic substrate has a CTE of 17 ppm/°C
- Capillary vs molded underfill vs no-flow



Underfill


Step I: Silicon, solder bump and substrate bond at reflow temperature (~230 C)
400 to 800 um die
Step II: Cool down from 230 C to room temperature
Step III: Underfilling, cure at 150 C, Cool to room temperature
Step IV: Lid attach/encapsulation at ~120C, cool down to room temp
Step V: Ball attach & reflow at ~ 230C,

Cu Pillar



- Foundation for most of future advanced packaging platforms
- Potential cost reduction for substrate
- Better electrical performance
- Better electromigration reliability than FC bump
- Larger die in a given body size

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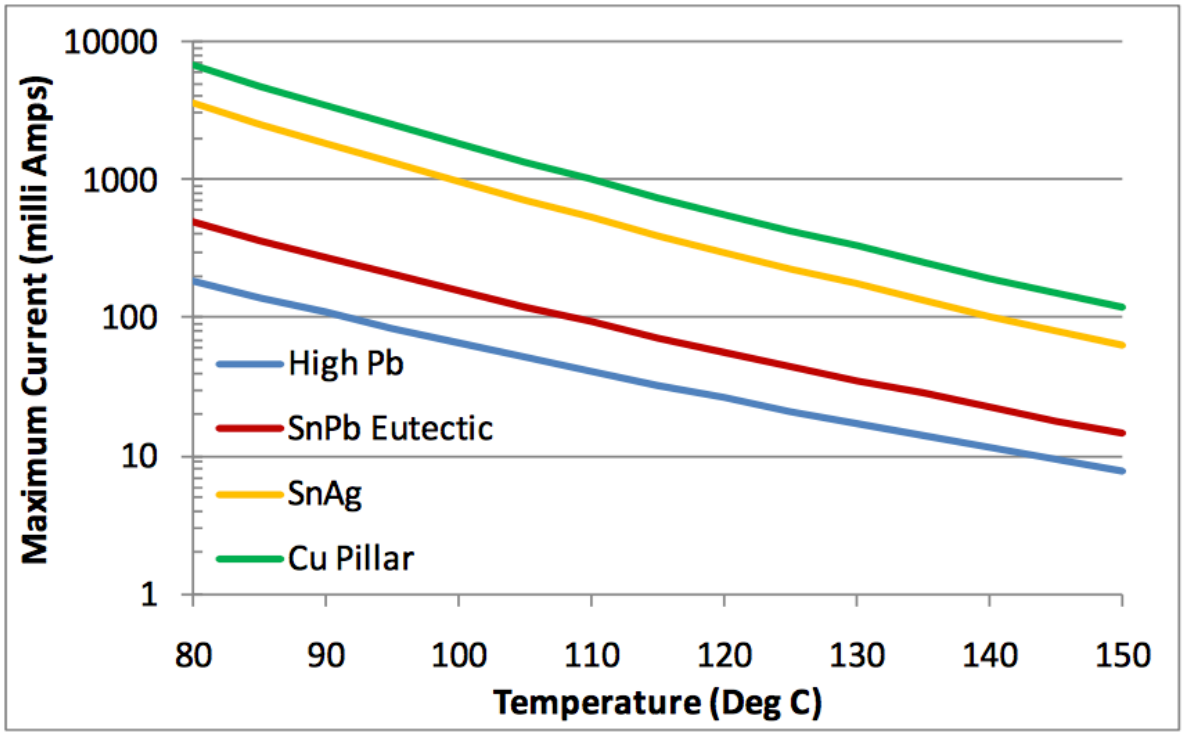
Maximum current carrying capacity (90um UBM diameter / 75um SRO diameter)

- 0.1% Failure rate at 100K Power On Hours (POH)
- For Cu pillar, no estimate for Black's Equation yet
  - Below estimate is based on comparison with SnAg for 150C/700mA condition



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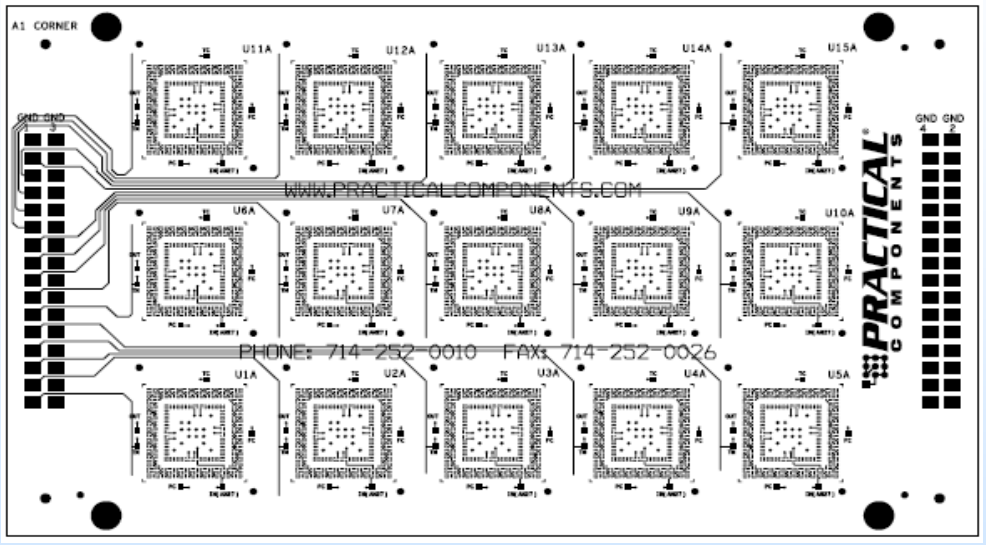
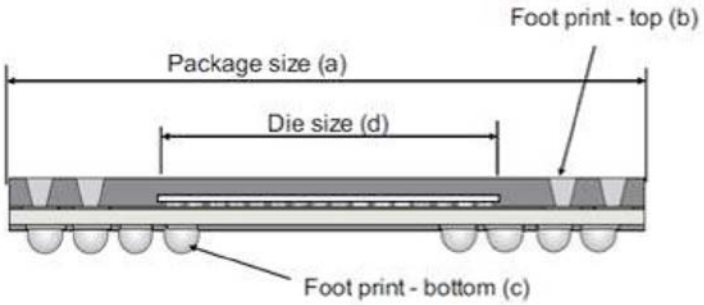
Package on Package and Solder Joint Encapsulants

- **BGA use in space applications will require interconnect package to board ruggedization**
  - **Options include capillary underfills, corner bonds, posts, staking, and no-flow underfill**
  - **Add complexity and yield issues to assembly**
- **Solder joint encapsulants are designed to enhance solder joint reliability and eliminate solder joint cracking**

Yincae Advanced Materials SMT 256



- PCB250-14-TMVDT-ENIG
  - (ENIG finished PWB)
- PCB250-14mm-TMVDT-ENEPIG
  - (ENEPIG finished PWB)
- PCB250-14mm-TMVDT-HASL
  - (Sn63 solder finished PWB).

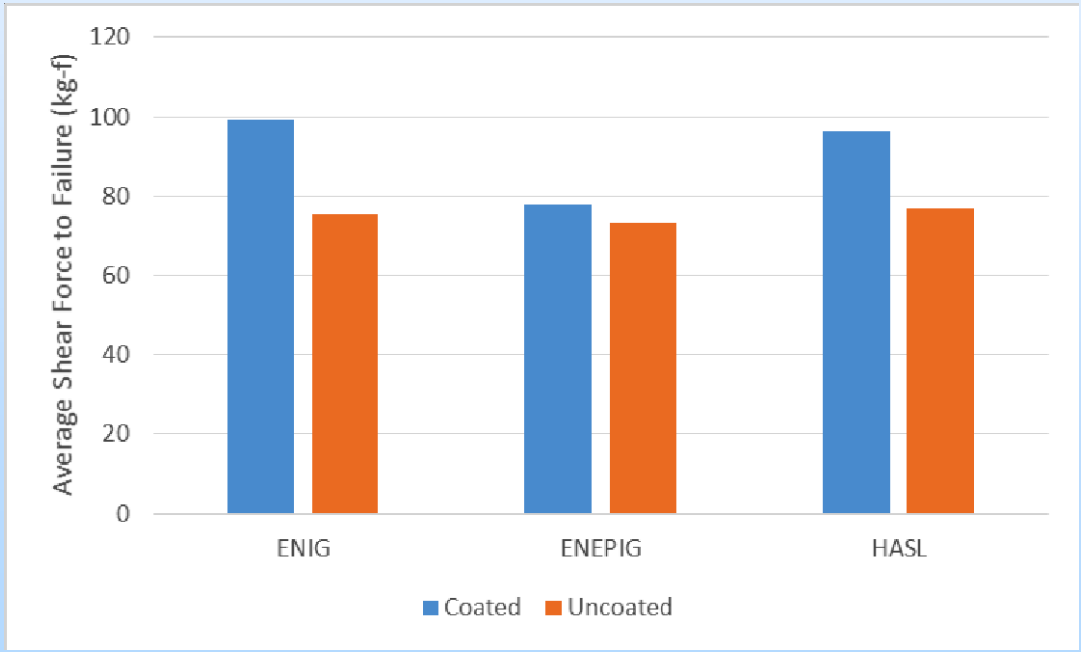


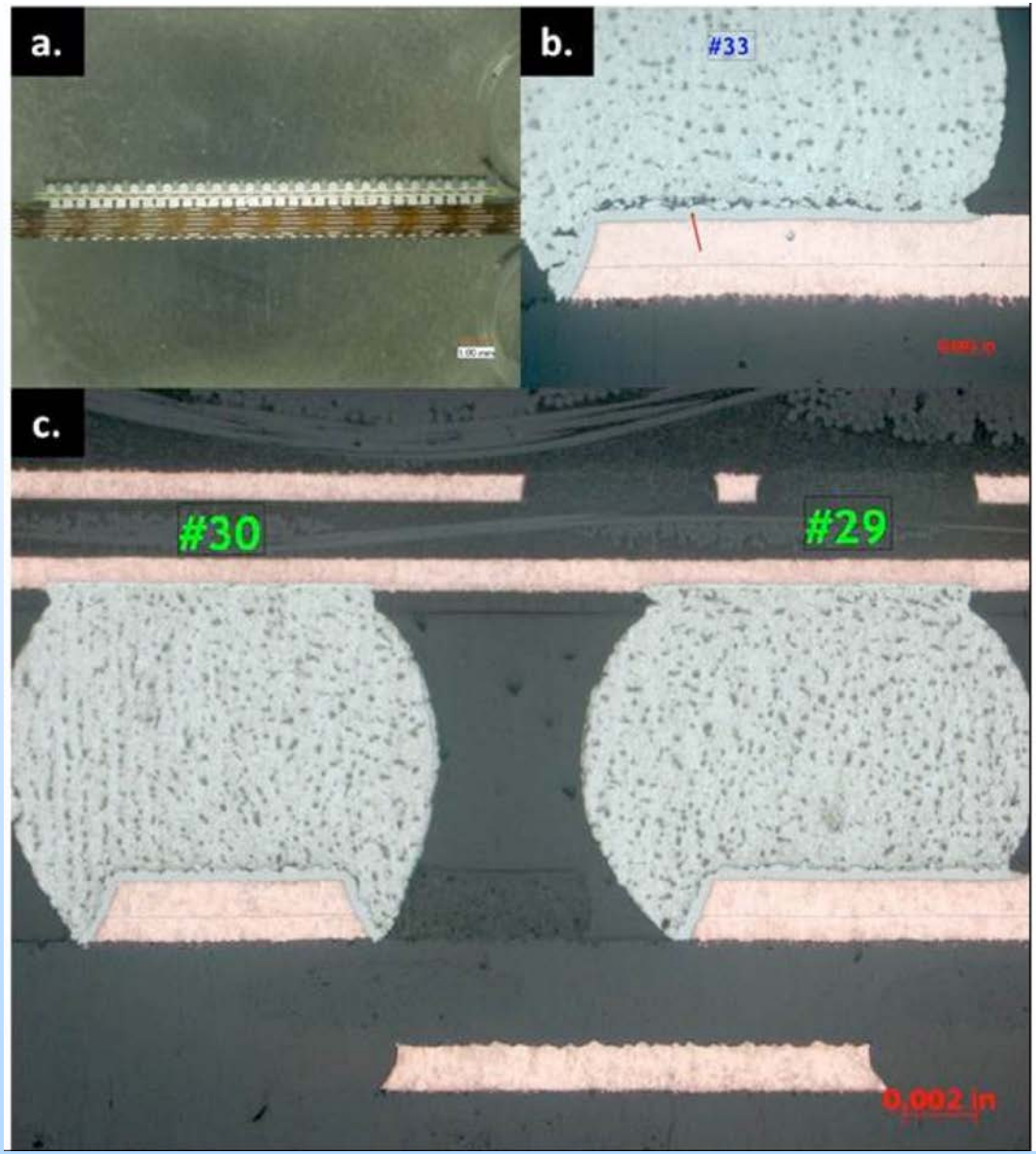
Body (a)	Foot Print–top (b)	Foot Print–bottom (c)	Die (d)
14 x 14mm	0.50 pitch, 200 ball 27 matrix, 2 row	0.4 pitch, 620 BGA 33 matrix, 4 + 2 row	7.6 x 7.6mm mm

Test Matrix

Substrates	PWB-HAZL (Qty. 4)		PWB-ENIG (Qty. 4)		PWB-ENPEG (Qty. 4)	
Component Attach	Sn63 (Qty. 3)	Sn63 + SMT256 (Qty. 3)	Sn63 (Qty. 3)	Sn63 + SMT256 (Qty. 3)	Sn63 (Qty. 3)	Sn63 + SMT256 (Qty. 3)
Processability	x	x	x	x	x	x
Reworkability	x	x	x	x	x	x
Solder Voids	x	x	x	x	x	x
Solder Open	x	x	x	x	x	x
Joint Cracking	x	x	x	x	x	x
Shear Test	x	x	x	x	x	x
Thermal Cycling (200 cycles; -55C to 125C)	x	x	x	x	x	x

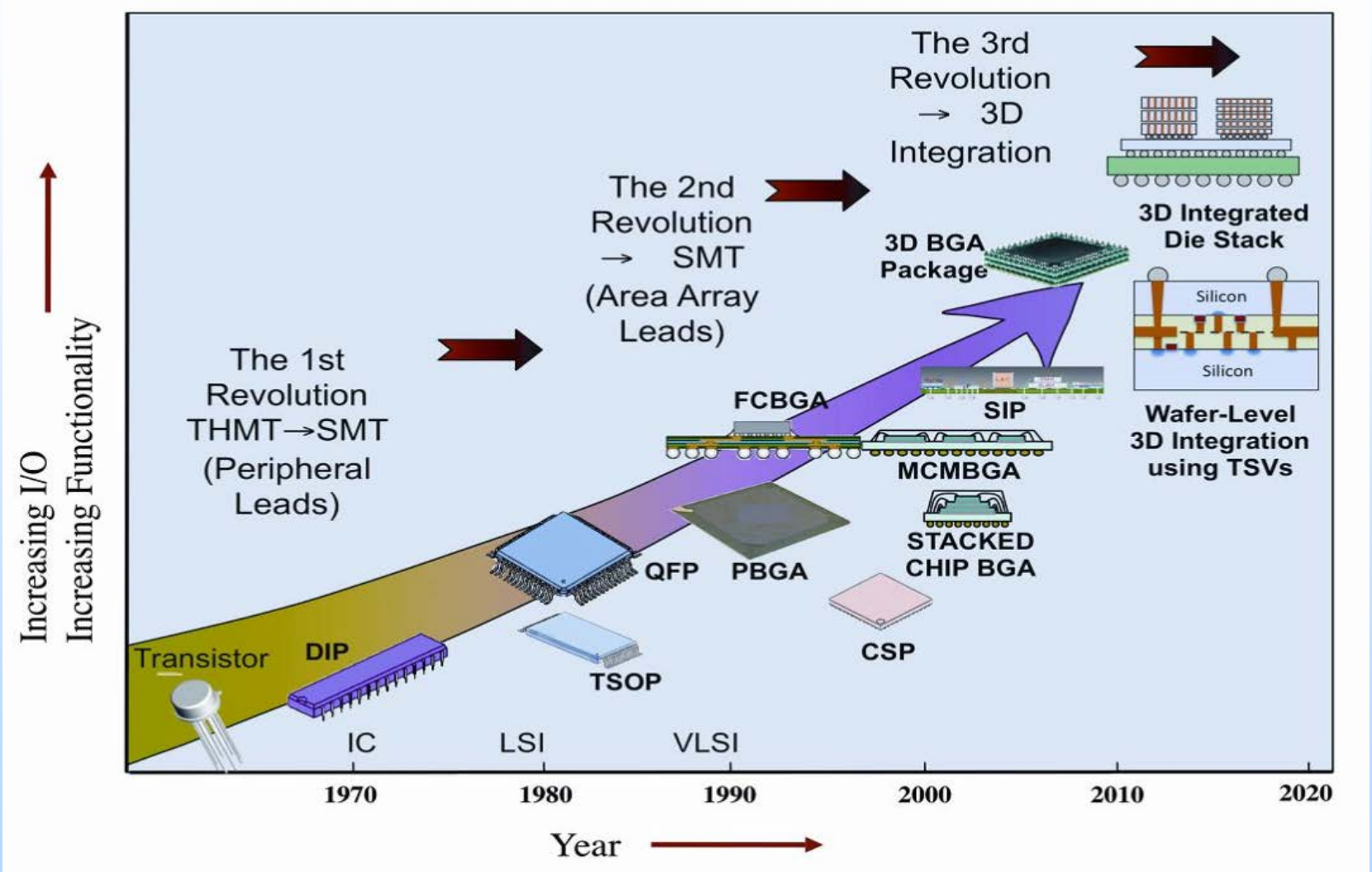
BGA solder joint encapsulant investigated showed signs of improving the strength of the solder joint and the solder joint reliability under thermal cycle conditions.



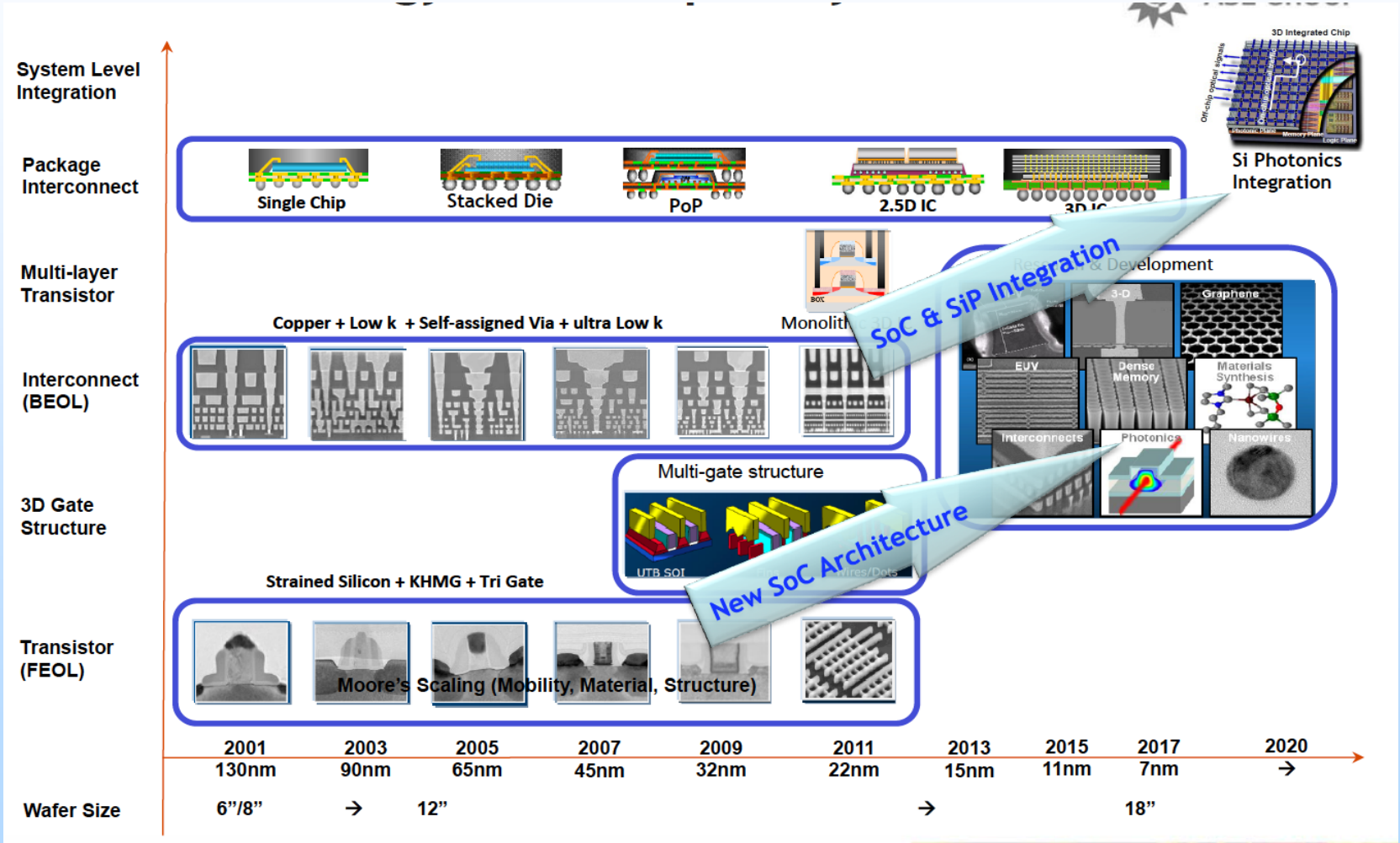


- Mounted and polished microsection of an ENIG finished assembly U8
- a) exhibiting solder cracks on ball #33
- b) No solder cracks are evident on the remaining solder balls evaluated, such as #29 and #30 (c).

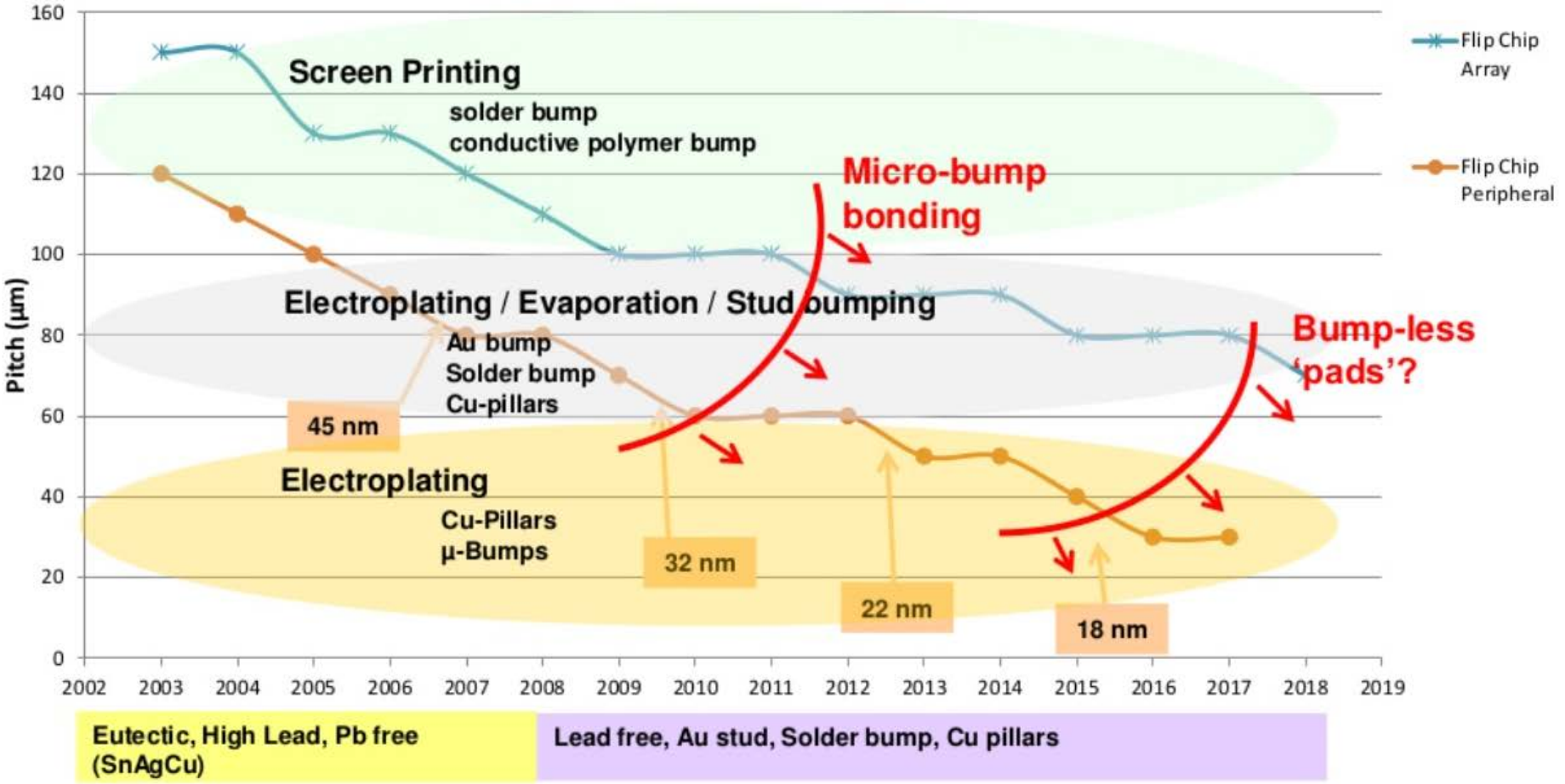
Packaging Roadmap

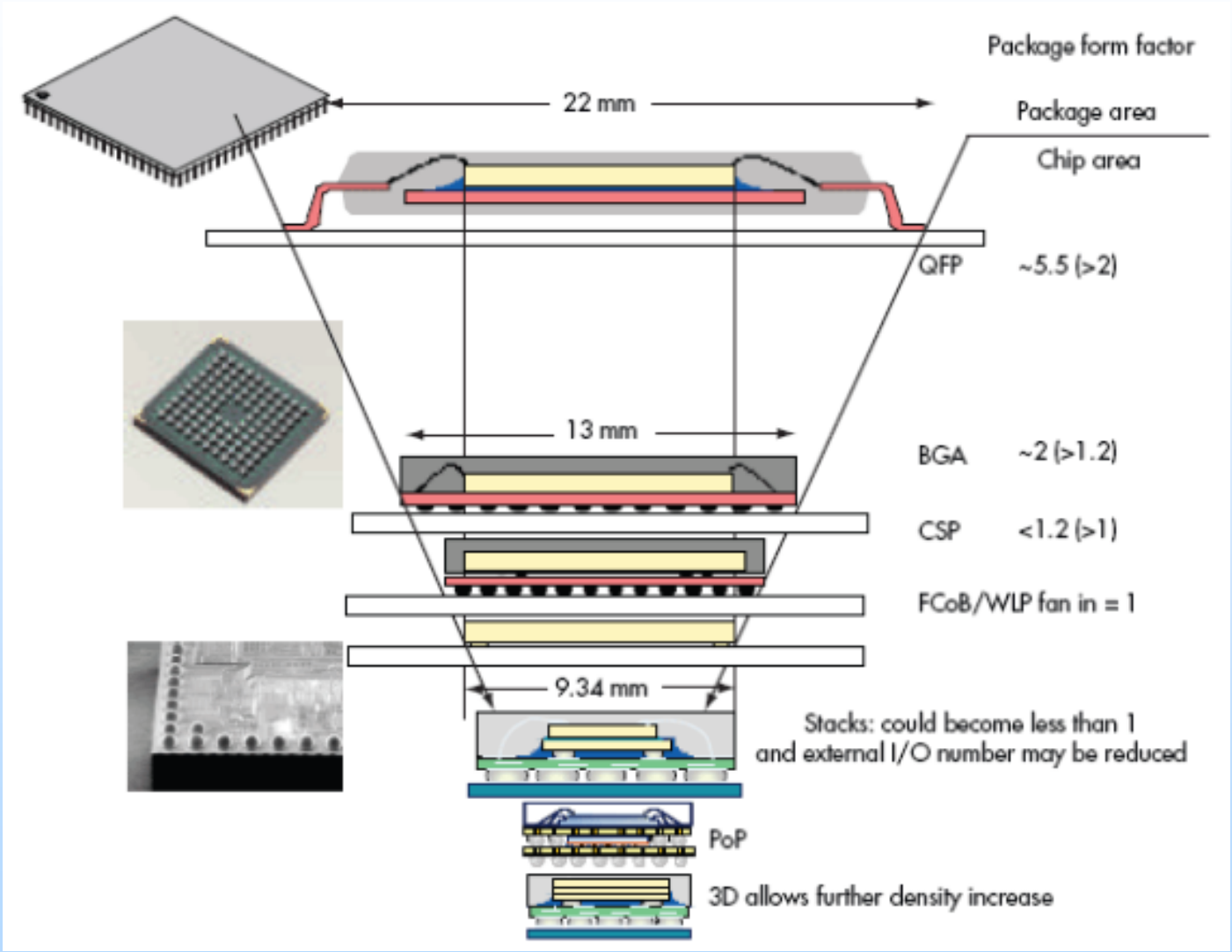


All Aspects of IC Technology Converging on 3D Processes

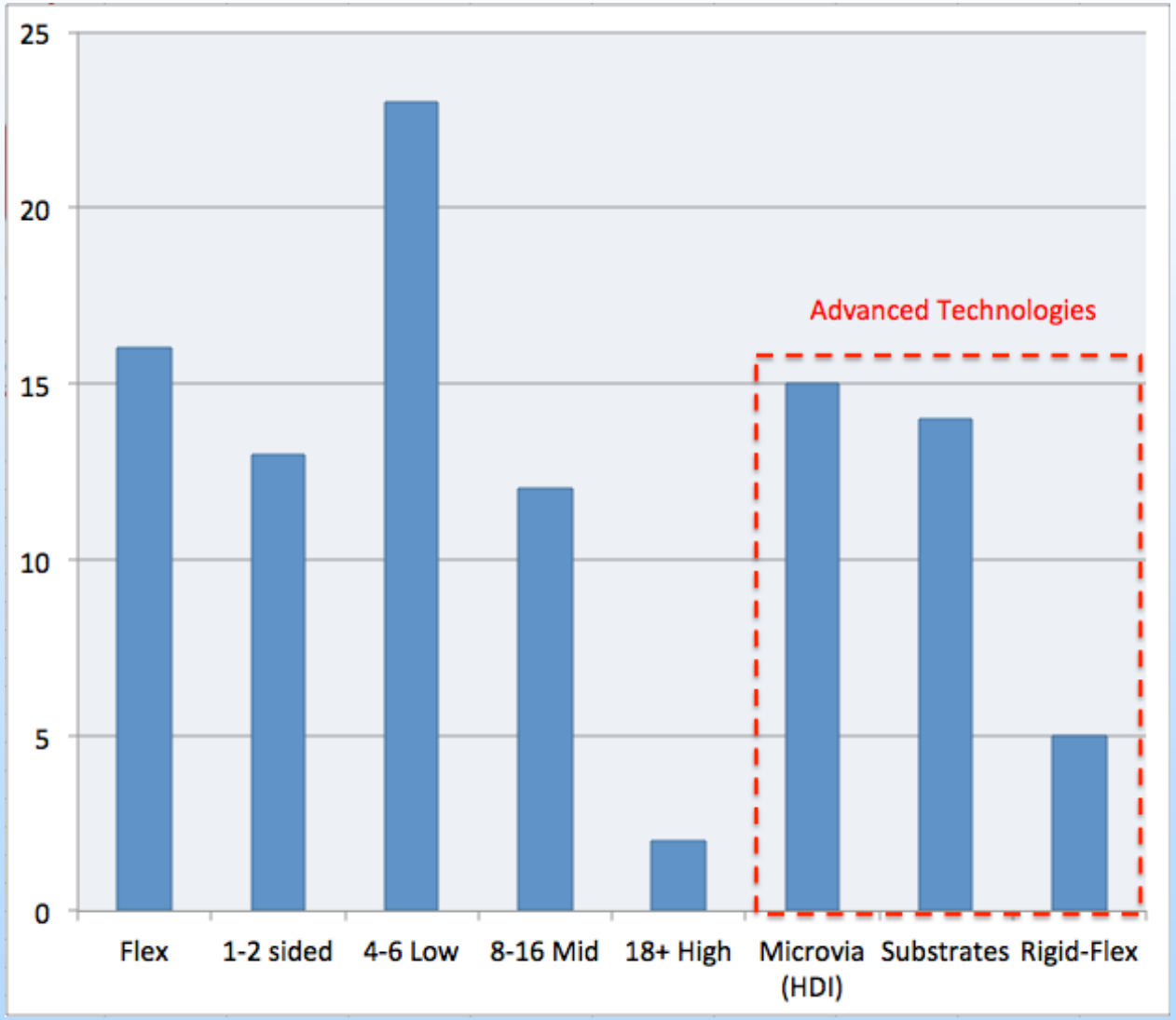


Bump Technology Roadmap

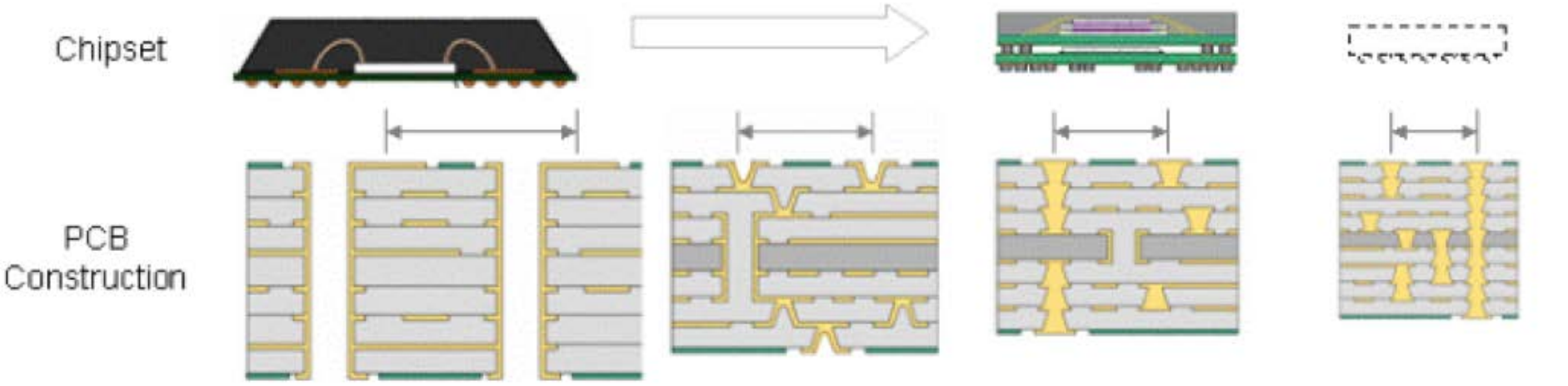



Package form factor
22 mm
Package area
Chip area
QFP
~5.5 (>2)
13 mm
BGA
~2 (>1.2)
CSP
<1.2 (>1)
FCoB/WLP fan in = 1
9.34 mm
Stacks: could become less than 1
and external I/O number may be reduced
PoP
3D allows further density increase

PCB Technology Market (2013)



High Density Interconnect Trends



Structure	Conventional	2+n+2 (6L)	3+n+3 (8L)	4+n+4, any-layer (10L)
Line & Space	100-125 µm	100-75 µm	100-75 µm	50-40 µm
Hole size	250-300µm	120-100µm	100-75 µm	75-50 µm
PCB Thickness	1.5 mm	1,0-0,9 mm	1,0-0,8mm	0,7-0,6 mm

Thank You